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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,934	07/15/2003	Yasuo Okada		6832

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,934	OKADA, YASUO	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 July 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure s 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5 and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al. (US 6,319,784).

In re claims 1-5, Yu et al. teach the claimed method of manufacturing method of a semiconductor device, comprising:

- forming a buried insulating film 12 in a semiconductor substrate 10 (Fig.1);
- forming semiconductor elements 14/16 isolated by the buried insulating film 12 (Fig.1);
- cleaning a surface side of the semiconductor substrate with a cleaning solution, i.e. using HF to clean native oxide 28 (col. 2, line 66 through col. 3, line 7); and

- covering a surface side of the buried insulating film 12 with a protective film 26 (silicon nitride) before the step of cleaning the surface side of the semiconductor substrate 10, wherein a protective film 26 is resistant to the cleaning solution.

In re claims 8-9, Yu et al. also teach a semiconductor device, comprising:

- a buried insulating film 12 which is formed in a semiconductor substrate 10;
- semiconductor elements 14/16 which are formed on the semiconductor substrate 10 and which are isolated by the buried insulting film 12; and
- a protective film 26 (silicon nitride) which covers all of a surface side of the buried insulating film 12 but which does not cover at least a region in which a salicide metal layer 32 of the semiconductor element is formed (Fig.6), wherein the protective film 26 is resistant to a hydrofluoric acid based solution (HF).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 7, 10 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. in view of Kuroda et al. (US 6,506,647).

In re claims 6 and 10, Yu et al. also teach forming a sidewall 20 (silicon nitride) on a side portion of a gate electrode 16 and wherein the sidewall 20 and the protective film 26 are the same material (silicon nitride) except that the gate electrode is of the MISFET.

However, the teachings of Yu et al. is a illustrative rather than restrictive (col. 4, lines 17-20). The semiconductor elements in Yu et al. are composed of gate electrode 16, gate insulating layer 14 and dielectric sidewall spacers 20, which is similar to the structure of MISFET, as evidenced by Kuroda et al. (Fig. 5), wherein Kuroda et al. teach MISFET Qn1 composed of gate insulating layer 8b, gate electrode 9a and dielectric sidewall spacers 12s (silicon nitride).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to apply the teachings of Yu et al. in MISFET of Kuroda et al. for a reasonable expectation of success because the semiconductor elements in both Yu et al. and Kuroda et al. are similar. By depositing the silicon nitride on the buried insulating film as the protecting layer, the buried insulating film would not suffer etching attack during the cleaning step.

In re claim 7, by applying the teachings of Yu et al. in forming MISFET, one of the ordinary skill in the art would have recognized that Yu et al. in view of Kuroda et al. also teach forming a salicide metal layer 32 on the gate electrode 16, a source diffusion region 22, and a drain diffusion region 22 (Fig.6 in Yu et al.) of the MISFET (i.e. when the semiconductor element in Yu is replaced by a MISFET) after the step of cleaning the surface side of the semiconductor substrate because the only difference is that Yu et al. do not expressly teach that the electrode 16 is an electrode of MISFET. However, this deficiency is remedy by Kuroda et al., as stated above.

With the combined teachings of Yu et al. and Kuroda et al., as stated above, the limitations as recited in claims 11-13 are also met because all limitations of claims 11-13 are same as that in claims 8-10.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Examiner
Art Unit 2823

March 17, 2004

Lee